ANALOG DEVICES

AN-634
APPLICATION NOTE

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ADN2830 Electrical Evaluation Kit

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INTRODUCTION

This application note describes the ADN2830 continuous wave laser driver Rev. A evaluation kit. The evaluation kit is a demonstration board that provides electrical evaluation of the ADN2830. This document describes how to configure the board in order to operate the ADN2830 electrically. The document contains the following information:

- Board description
- Board settings description
- Choosing the external components and board configuration
- Quick start for electrical operation
- Component list
- Schematic of board
- Board layout information
- Silkscreen image of board
- Design examples

BOARD DESCRIPTION

The ADN2830 is a continuous wave (CW) laser driver that provides closed-loop control of the average power after calibration over time and temperature. When it is used in conjunction with a laser, a monitor photodiode (MPD) current is required to control the power in the laser. The MPD current is fed into the ADN2830 to control the average power.

To use the board in an electrical configuration, a current mirror circuit is employed to close the average power loop. The board is initially set up to divide the bias current by 200, thus producing the simulated monitor photodiode current. The ADN2830 evaluation board can provide up to 200 mA bias current in standalone mode and up to 400 mA if two ADN2830s are used in current booster mode. The board also has the option to choose between sinking and sourcing the bias current. The LEDs for power supply, DEGRADE, and FAIL are made available for monitoring purposes.

Power to the evaluation board is 5 V only.

Table I. Board Settings Description

Component	Name	Function
K1		Jumper to Bypass Supply Protection Diode
K2	MODE	Jumper to set U2 in Standalone Mode (A) or Current Booster Mode (B)
K5	ALS	Jumper to Exercise ALS (When Inserted, the Laser Is Turned Off)
K6		Enables Current Sourcing Circuitry when Inserted
J3	Power	5 V Power Input to Board
T1, T2		Measures the BIAS Current in Current Sinking Mode
T3		Bias Current Mirror Monitor
T5, T6		Measures the Current Provided by the ADN2830 in Current Sourcing Mode
T7, T8		Measures the BIAS Current in Current Sourcing Mode
T13		IMPD Current Mirror Monitor

CHOOSING THE EXTERNAL COMPONENTS AND THE BOARD CONFIGURATION

To set up the board, the user should follow these steps:

1. Establish the Current Range

The default configuration of the board allows the user to program currents up to 200 mA. When currents greater than 200 mA are required, the MODE function allows the user to operate multiple ADN2830s in parallel current boosting mode. The ADN2830 evaluation board has an option to mount a second ADN2830, U2 (not populated in the original board configuration). In this configuration, the user can establish currents as large as 400 mA. When both U1 and U2 are on the board, the desired configuration is established by switch K2 (See Table II).

Table II. K2 Switch Positions

Maximum Bias Current	Position of K2
200 mA (standalone mode)	A
400 mA (current booster mode)	B

Note that when both U1 and U2 are on board and K2 is in position A, the current taken from the supply will be greater than in the case with only U1 on board.

2. Set the Bias Current Sinking/Sourcing Mode

The ADN2830 may be employed in either current sink mode or current source mode. The default configuration is in current sink mode, and the PNP current mirror (Q1 and Q2) is used to close the average power loop, and thus, takes the place of the laser and monitor photodiode. Mirror gain is related to laser slope efficiency and monitor photodiode current. The board is initially set up to divide the bias current by 200. To use the ADN2830 in current source mode, components U3, Q5, and Q6 should be populated. In this case, K6 should be inserted. Also, the user should remove R8 and R35 and populate R20 and R22. The current sourced by Q6 is given by the following formula:

$$I_S = IBIAS \times \frac{R20 \| R22}{R12 \| R14 \| R17 \| R18} \quad (1)$$

where:

IBIAS is the bias current provided by the ADN2830 (maximum 200 mA/400 mA).

I_S is the source current required.

To close the control loops, Q5 and Q6 are connected in a current mirror configuration. The gain of the mirror is given by the ratio

$$\left(R12 \| R14 \| R17 \| R18\right) / R7$$

When choosing the components, the user should take care to avoid the compliance voltage breaking at the IBIAS pin.

Note that the current mirror circuitry does not simulate the laser threshold current.

3. MPD Configuration

Care should be taken when choosing the current mirror gain to ensure that the current applied to the IMPD pin when used is within the data sheet specifications (50 μA to 1200 μA). When MPD currents are anticipated to exceed 1.2 mA, the IMPD block may be bypassed and the control loop can be closed by connecting the MPD anode to the PSET node directly. This allows the user to have MPD currents as large as 8 mA (See Table III).

Table III. IMPD Block Usage

Configuration	R25/R31*	R26/R30*	R28
IMPD Block Used	Not Populated	0 Ω	Not Populated
IMPD Block Bypassed	0 Ω	Not Populated	0 Ω

* In sink current mode, R25 and R26 are used. In source current mode, R30 and R31 are used.

4. Calculate Values for R19 and R21 (PSET and ASET)

The average power is given by the value of the PSET potentiometer (R21). The average power control loop will servo the PSET pin to approximately 1.23 V. When using the electrical evaluation board, it is easy to compute and program a desired value of *IBIAS*. The following formula allows the user to calculate the approximate values of R_{PSET} for a desired *IBIAS*:

$$R_{PSET} = \frac{1.23\,V}{IBIAS \times G} \quad (2)$$

where *G* is the current mirror gain.

$G_{SINKING\ MODE}$ = (R34 || R5 || R4 || R6)/R2

$G_{SOURCINGMODE}$ = (R12 || R14 || R17 || R18)/R7

R_{PSET} is the total resistance at the PSET pin (R21 + R33).

When using the board in current sourcing mode, the bias current from Equation 2 should be replaced with the sourcing current I_S (see the relation from Step 2).

The alarm threshold level can be adjusted with R19. It can be calculated with the following formula:

$$R19 = N \times \frac{1.23\,V}{I_{FAIL}} \times 200 \quad (3)$$

where:

I_{FAIL} is the bias current value, which will raise the fail alarm.

N is the number of ADN2830s used.

In the current sourcing mode, the user should calculate the bias current (the alarm threshold level) from I_S using relation 1. The DEGRADE alarm will be raised when the bias current reaches 90% of I_{FAIL}. The total resistance at the ASET pin should be within the range 1. 2 kΩ to 13 kΩ. R32 ensures that it will not be shorted to ground. If the resistance exceeds 13 kΩ, the ADN2830 may not operate within specifications.

In the board default configuration, R32 = R33 = 100 Ω and R19 = R21 = 50 kΩ. For high currents, it may be necessary to reduce these values to ensure more accurate adjustments for the bias current and alarm threshold level.

IMPORTANT: When choosing the components from the current mirrors (resistors and transistors), care should be taken not to exceed the maximum power dissipation.

QUICK START FOR ELECTRICAL OPERATION

1. Choose the jumper settings for the desired configuration. (The default configuration is sinking current mode, standalone, bypassing the IMPD block.)
2. Adjust R19 and R21 to the calculated values.
3. Connect the power supply and adjust R21 to obtain the desired value for IBIAS.
4. Check the voltage at the cathode of D1 to be within the range of 4.5 V to 5.5 V and then check the voltage compliance condition at the IBIAS pin (1.2 V < V_{IBIAS} < VCC). If one or both of these conditions are not met, then the user should redesign the external circuitry. (Choose degeneration resistors with smaller values in the current mirror used.)
5. The ADN2830 has fully integrated monitoring features of IBIAS and IMPD at the IBMON and IMPDMON pins (T3 and T13). In current sourcing mode, the user should take into account the ratio between the bias current given by the ADN2830 and I_S when using the bias current monitoring function.

Table IV. Component List

Component	Value/Description	Quantity/ Board
R1, R9, R16	330 Ω SMD Resistors	3
R15, R10, R3, R11, R13	1 kΩ SMD Resistors	5
R19, R21	50 kΩ SMD Trim Pots	2
R32, R33	100 Ω SMD Resistors	2
R2	2.2 kΩ SMD Resistor	1
R4, R5, R6	33 Ω SMD Resistors	3
R8	1 Ω SMD Resistor	1
R25, R28	0 Ω SMD Resistors	2
R29, R27, R24, R23, R20, R22, R26, R30	Not Populated	
R31, R7, R34, R12, R14, R17, R18, R35	Not Populated	
C1	22 μF SMD Capacitor	1
C2	220 μF SMD Capacitor	1
C8, C9, C10, C11, C12	10 nF SMD Capacitors	5
C14	1 μF SMD Capacitor	1
L1	10 μH SMD Inductor	1
K1, K5	2-Pin Headers	2
K2	3-Pin Header	1
K6	Not Populated	
J3	SMA Side-Launch Connector	1
D1	1N4001 Diode Plastic Package	1
D2, D3, D4	SMD LEDs	3
Q3, Q4	SOT-23 Transistors	2
Q1, Q2	BC327	2
Q5, Q6	Not Populated	
U1	ADN2830	1
U2	ADN2830— Not Populated	1
U3	AD820 SOIC Package— Not Populated	1

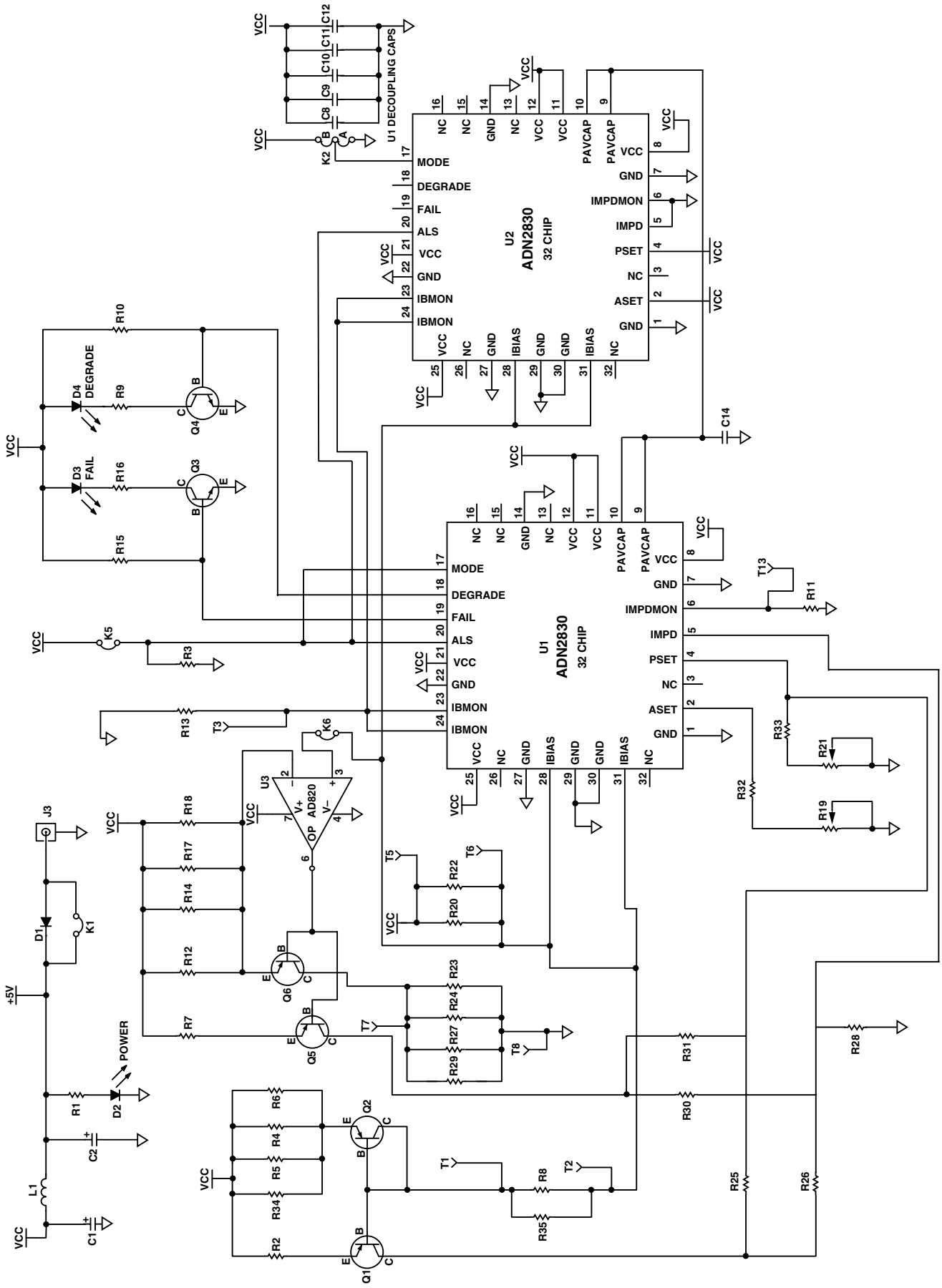

Figure 1. Schematic of Board

BOARD LAYOUT

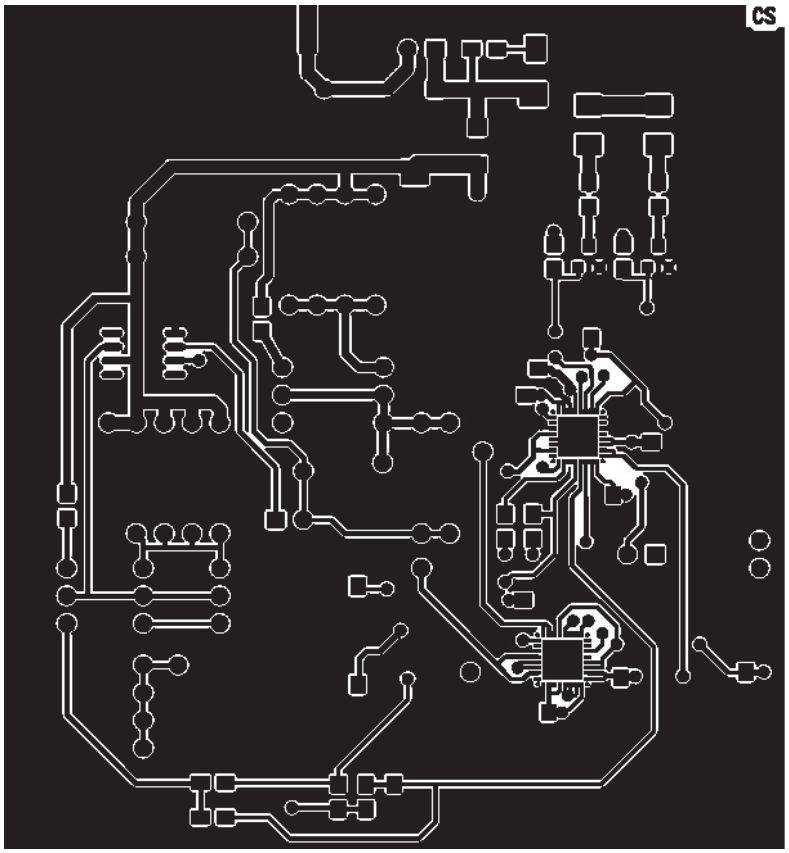

Figure 2. Component Side

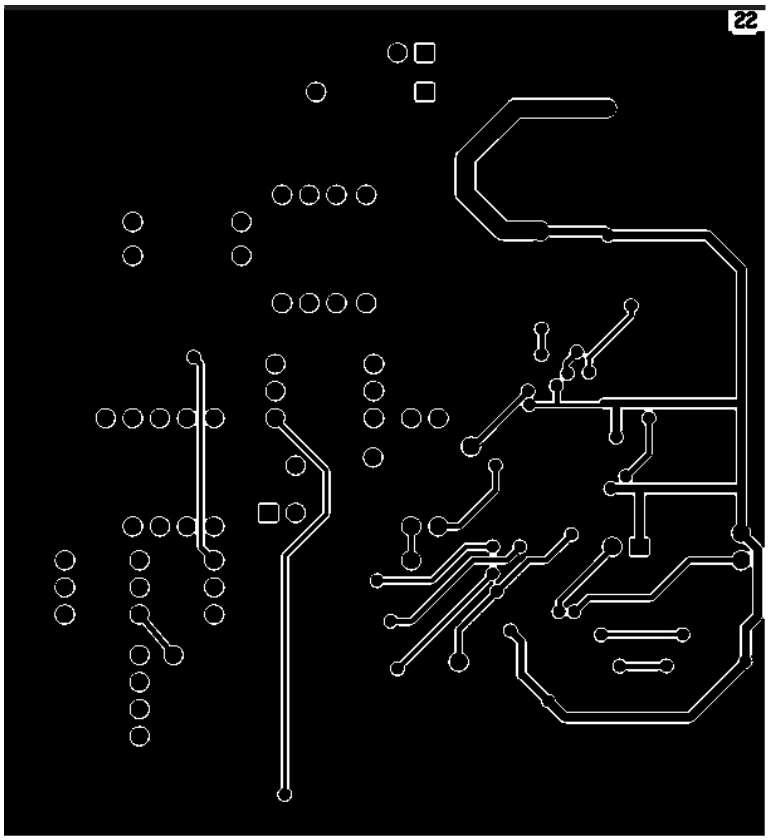

Figure 3. Solder Side

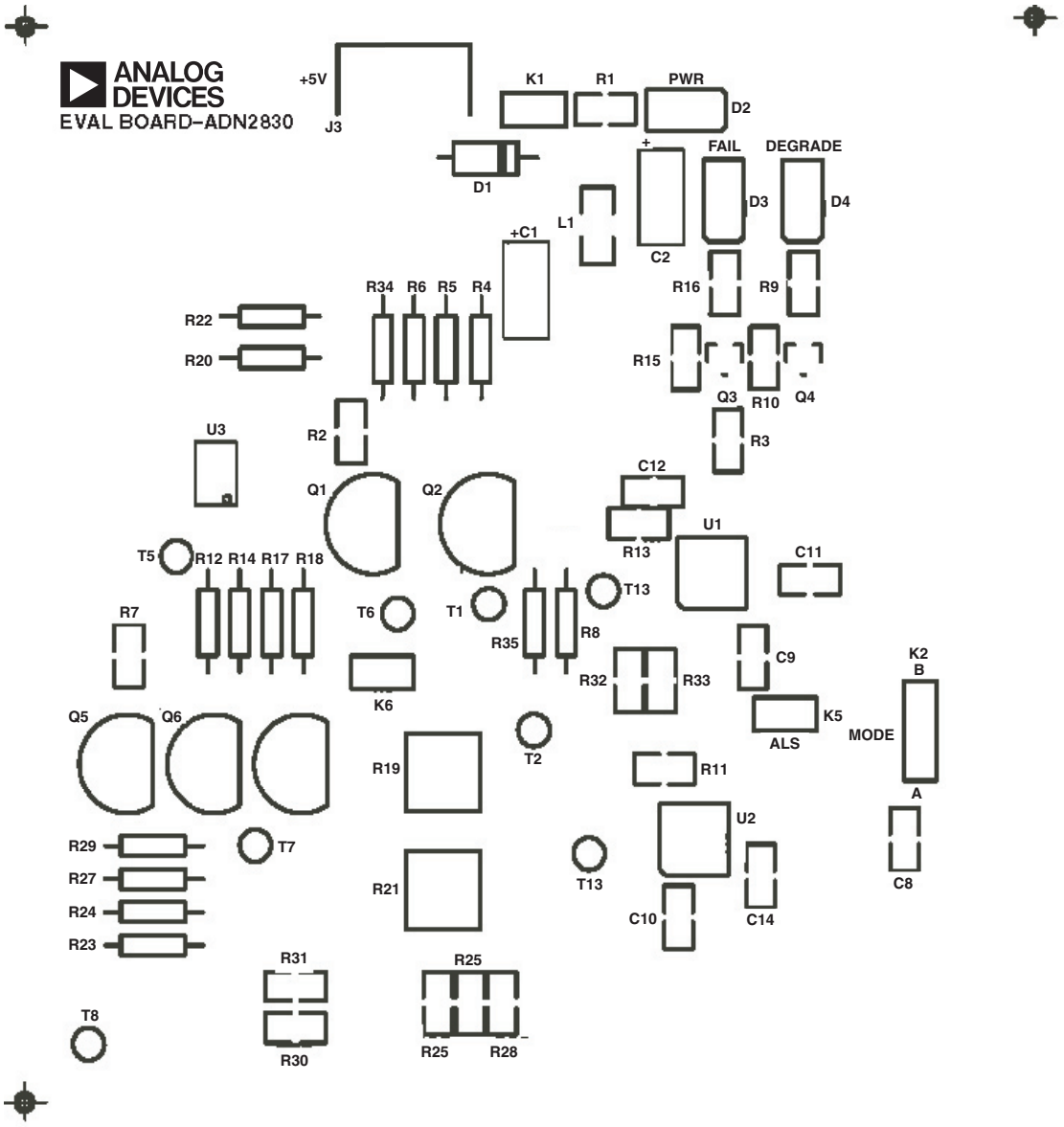

Figure 4. Silkscreen Image

DESIGN EXAMPLES

This section describes two design examples that cover both current source and sink modes. When designing the external circuitry, the user should establish the desired range for the bias current. If it is necessary to use the IMPD block, care should be taken in choosing the current mirror gain to ensure that the IMPD current will be within the range 50 μA to 1200 μA and the voltage on the IBIAS pin > 1.2 V. When the IMPD block is not used, there are no major restrictions in choosing the current mirror gain. In the following examples, the current mirror gain will be 1/200, but the user should change this value to fit other individual needs. The following calculations are for the single ADN2830 option. If more than one ADN2830 is used, the current mirror gain must be changed in order to ensure that the parts are working within data sheet specifications (IMPD current and IBIAS compliance voltage).

Example 1: Current Sink Mode

Considering the current mirror gain equal with 1/200, the bias current can be adjusted between:

- 10 mA to 200 mA when using the IMPD block
- 4 mA to 200 mA (full range) when bypassing the IMPD block (connecting directly to PSET node)

The lowest value of bias current achievable is determined by the minimum value of IMPD current and the current mirror gain and the highest value is limited by the ADN2830 (200 mA). This value may be increased by connecting more ADN2830s in parallel. Assuming that V_{BE} = 0. 7 V and V_{IBIAS} = 2 V (>1. 2 V), then for the highest bias current (200 mA), the following formula allows the user to calculate the values for the resistors from Q2's collector, R8 and R35:

$$\left(R34 \left\| R5 \right\| R4 \left\| R6\right)+\left(R8 \left\| R35\right)=\right.$$

$$\frac{V_{CC}-V_{BE}-V_{IBIAS}}{I_{BIAS\,max}}=\frac{5-0.7-2}{0.2}=11.5\,V$$

where:

R35 and R34 are not populated and R8 = 1 Ω ≥ R34||R4||R5||R6 = 10 Ω. One possible solution is R4 = R5 = R6 = 30 Ω.

The current mirror gain is given by the following formula:

$$\frac{\left(R34 \left\| R5 \right\| R4 \left\| R6\right)\right.}{R2}=\frac{1}{200}$$

As a result, $R2$ = 10 Ω × 200 = 2 kΩ

R_{PSET} is given by the formula:

$$R_{PSET}=\frac{1.23\ V}{IMPD}$$

$R_{PSET\ min}$ is calculated when ADN2830 is sinking N × 200 mA, where N is the number of ADN2830s in parallel.

Assuming that the current mirror provides 1 mA through R_{PSET} at the highest bias current, then $R_{PSET\ min}$ = 1. 2 kΩ.

The value for $R_{PSET\ max}$ is:

$R_{PSET\ max}$ = 1. 23 V/0. 05 mA = 24.6 kΩ

As a result, R21 = $R_{PSET\ max}$ and R33 = $R_{PSET\ min}$.

The mechanical trimpots used on this evaluation board are 11-turn potentiometers. These potentiometers may limit the user's ability to finely adjust values of bias current. In practical applications, the ADN2850, a 10-bit digital potentiometer, is recommended.

Example 2: Current Source Mode

In this mode, Q5 and Q6 are connected as a current mirror. The values for R7, R12, R14, R17, and R18 may be calculated in the same manner as the previous example, considering the bias current as the current needed to be sourced. If the current sourced range is the same as the current sink range from the previous example, then R7 = R2, R5 = R4 = R3 = R12 = R14 = R17, and R18 is not populated. The current mirror gain gives the ratio between the MPD current and the current sourced.

Assuming that at saturation $V_{CE} = V_{BE}$ = 0. 7 V, the following formula allows the user to calculate the equivalent resistance connected to the collectors of Q6 (R29||R27||R24||R23):

$$\left(R29 \left\| R27 \right\| R27 \left\| R23\right)\right. \le$$

$$\frac{V_{CC}-V_{CE}-I_{IBIAS\,max}\times\left(R12 \left\| R14 \right\| R17 \left\| R17\right)\right.}{I_{BIAS\,max}}$$

Considering now the effect of the operational amplifier, the ratio between the sourced current and the bias current provided by ADN2830 is given by

$$\frac{IBIAS}{I_{ADN2830}}=\frac{\left(R20 \left\| R1\right)\right.}{R12 \left\| R14 \right\| R17 \left\| R18}$$

Therefore, it is possible to source currents greater than 200 mA using only one ADN2830.

In both current sinking and sourcing modes, the alarm threshold will be established by the resistance connected to the ASET node. The threshold represents the bias current value that will raise the FAIL alarm. When the bias current reaches 90% of the threshold value, the DEGRADE alarm is raised. In the sink current mode, the resistance needed to set the threshold may be calculated with the formula

$$R19=N\times\frac{1.23\ V}{I_{FAIL}}\times 200$$

where:

N is the number of ADN2830s connected in parallel.

I_{FAIL} is the bias current provided by the *N* ADN2830s, which will raise the FAIL alarm.

When the current source option is used, I_{FAIL} from the above formula is obtained by multiplying the current sourced by Q6 and Q7 with the following ratio.

$$\left(R12 \left\| R14 \right\| R17 \left\| R18\right)\right) / \left(R20 \left\| R22\right)\right)$$

When choosing the resistors from the current mirror, users should take into account that they have to dissipate $P = I^2 \times R$. In the mean time, Q2 and Q6 should be able to provide the required current, and the total power dissipated on these transistors should not exceed their data sheet specifications.

$$P_{DATA\ SHEET} >> \frac{V_{CCmax} \times I_{Cmax}}{4}$$

where:

$V_{CC\ max}$ is the maximum supply voltage.

$I_{C\ max}$ is the maximum collector current required.

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